Please amend the claims as follows (this listing replaces all prior listings):

1-20. (Cancelled).

21. (Currently amended) An apparatus comprising:

drain-source connected MOSFET capacitors, each capacitor selectable by an independent control signal generated by a logic circuit, the selected capacitors to provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors; ~~and~~

buffer circuitry for decoupling the capacitors from the logic circuit to prevent noise in the logic circuit from affecting the capacitors; and

a low pass filter connected to a DC power supply to generate a bias voltage to bias the drains and sources of the MOSFET capacitors.

22. (Currently amended) The apparatus of claim 21, ~~further comprising a filter circuit connected to a power supply to generate a filtered power supply signal that is used to power~~ in which the bias voltage also powers the buffer circuitry.

23. (Previously presented) The apparatus of claim 21, further comprising transmission gates, each of which corresponds to one of the capacitors and can be turned on by the independent control signal when the corresponding capacitor is selected.

24-27. (Cancelled).

28. (Previously presented) The apparatus of claim 23 in which a node of each of the transmission gates is connected to a gate node of the corresponding MOSFET capacitor.

29-30. (Cancelled)

31. (Previously presented) The apparatus of claim 21, wherein each of a subset of one or more of the MOSFET capacitors comprises a P type enhancement mode MOSFET.

32. (Cancelled)

33. (Previously presented) The apparatus of claim 21, wherein each of a subset of one or more of the MOSFET capacitors comprises an N-type depletion mode MOSFET.

34. (Previously presented) The apparatus of claim 21 in which at least one of the MOSFET capacitors has a capacitance that is less than 1 pF.

35. (Currently amended) An apparatus comprising:

on-chip capacitors disposed on an integrated circuit, each capacitor selectable through an independent control signal ~~generated by a logic circuit~~, the selected capacitors to provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors~~,~~ ~~each capacitor comprising at least one of an on-chip metal capacitor and an on-chip poly capacitor~~; ~~and~~

transmission gates, each corresponding to one of the capacitors and can be switched on by the independent control signal to select the corresponding capacitor;

a logic circuit to generate the control signals for switching on a subset of the transmission gates to select a corresponding subset of the capacitors, the logic circuit having sufficient driving power to switch the transmission gates; and

buffer circuitry for decoupling the ~~capacitors~~ transmission gates from the logic circuit to prevent noise in the logic circuit from affecting the selected capacitors.

36. (Previously presented) The apparatus of claim 35, further comprising a low pass filter connected to a power supply to generate a filtered power supply signal that is used to power the buffer circuitry.

37-38. (Cancelled)

39. (Currently amended) A method comprising:

selecting a subset of a plurality of drain-source connected MOSFET capacitors to provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors, the selecting including using a logic circuit to generate control signals to select the subset of capacitors; ~~and~~

decoupling the capacitors from the logic circuit by using a buffer circuitry to prevent noise in the logic circuit from affecting the plurality of capacitors; and

using a low pass filter connected to a DC power supply to generate a bias voltage to bias the drains and sources of the MOSFET capacitors.

40. (Currently amended) The method of claim 39, further comprising ~~generating a filtered power supply signal, by using a low pass filter,~~ using the bias voltage to power the buffer circuitry.

41-42. (Cancelled)

43. (Previously presented) The method of claim 39 in which each of a subset of one or more of the MOSFET capacitors comprises a P-type enhancement mode MOSFET.

44. (Previously presented) The method of claim 39 in which each of a subset of one or more of the MOSFET capacitors comprises an N-type depletion mode MOSFET.